Capacitance Coupling Immune, Transient Sensitive Accelerator for Resistive Interconnect Signals of Subquarter Micron ULSI

Tomofumi Iima, Masayuki Mizuno, *Member, IEEE*, Tadahiko Horiuchi, and Masakazu Yamashina, *Member, IEEE*

Abstract—**This paper presents a new circuit scheme called a transient sensitive accelerator (TSA) circuit for highly resistive interconnects. The TSA can reduce both delay time and crosstalk voltage. Using the TSA with an interconnect length of 30 mm reduces delay time and crosstalk voltage by 29% and 20%, respectively. A further advantage is that the TSA operates in self-time and thus can be applied to bidirectional signal communication.**

I. Introduction

UNTIL recently, gate delay was a major factor determining the overall delay on a chip, and interconnect delay was a minor factor. However, because of the decrease in the minimum feature size, global interconnect delay is becoming more important and gate delay is losing importance [1]. In addition to delay, reducing the feature size causes another serious problem, i.e., crosstalk. As interconnect minimum spacing and width continues to decrease, the aspect ratio of the interconnect wires must be increased to keep the wire resistance low. This, in turn, leads to an increase in the parasitic capacitance between interconnects. These problems may eventually make interconnect performance a limiting factor in overall large scale integration (LSI) performance.

Fig. 1 shows a projection of the cycle time of an LSI, and the number of gates on the chip when the minimum feature size decreases. We assume there are three interconnect layers, and that the die size is 30 mm by 30 mm at each feature size. The reason the cycle time increases even though the minimum feature size continues to decrease is because the global wire delay is becoming a limiting factor in the overall delay. As is clear from the figure, global interconnect delay represents a dominant factor in 0.15-μm technology.

Various methods of reducing interconnect degradation have been investigated. These include replacing the aluminum used in interconnects with less resistive metals such as copper and using substances with a lower dielectric constant as interlevel dielectric materials. It has been found that inserting repeaters is an effective way of reducing the delay time. This method, however, cannot be applied to bidirectional signal lines, since it requires a separate control signal.

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T. Iima, M. Mizuno, and M. Yamashina are with the Microelectronics Research Laboratories, NEC Corporation, Sagamihara, Kanagawa, 229, Japan.

T. Horiuchi is with ULSI Device Development Laboratories, NEC Corporation, Sagamihara, Kanagawa, 229, Japan.

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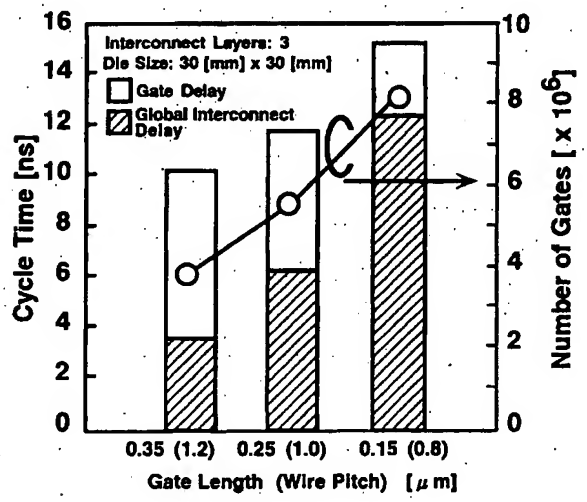


Fig. 1. Projection of cycle time and gate count.

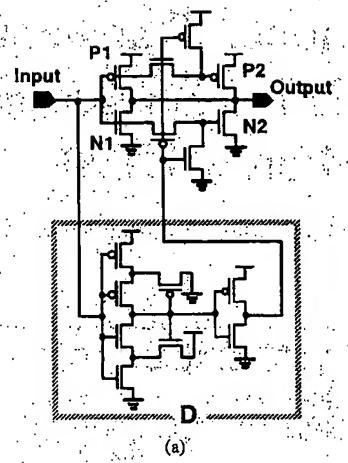
We assume a circuit model with an interconnect linking the circuit driver and receiver. The driver resistance R_D, the resistance and capacitance of the interconnect, R_{int} and C_{int}, and receiver capacitance C_R are the key points in this driving scheme model. When R_{int} is negligibly small, enhancing the current drive capability by enlarging the drive size effectively reduces the overall delay. However, if R_{int} becomes comparable to or larger than the R_D, enlarging the driver size is no longer effective. Thus, to reduce the delay, we have to focus on the receiver or interconnect, rather than on the driver.

As a means of reducing delay time, we have developed a new receiver circuit which we call the transient sensitive trigger (TST) circuit. We have also developed another circuit, transient sensitive accelerator (TSA) circuit, which can reduce both delay and crosstalk. The former is used as a subcircuit in the latter. Delay time and crosstalk voltage are reduced by 29% and 20%, respectively, with the newly-developed TSA circuit.

II. Transient Sensitive Trigger (TST) Circuit

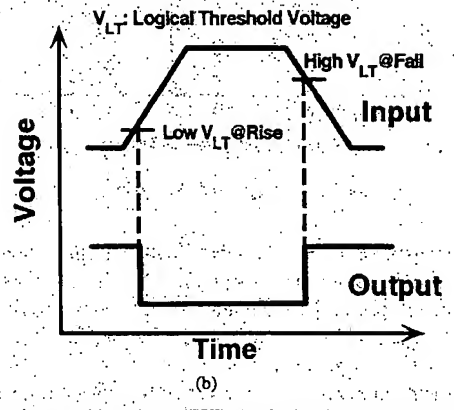
A. Operation

To replace the conventional inverter which is normally used as a receiver, we developed the TST circuit shown in Fig. 2(a). The advantage of the TST circuit is that it can reduce



(a)

transistor	W [um]	L [um]
P1	1.6	0.25
N1	1.6	0.25
P2	32.0	0.25
N2	16.0	0.25

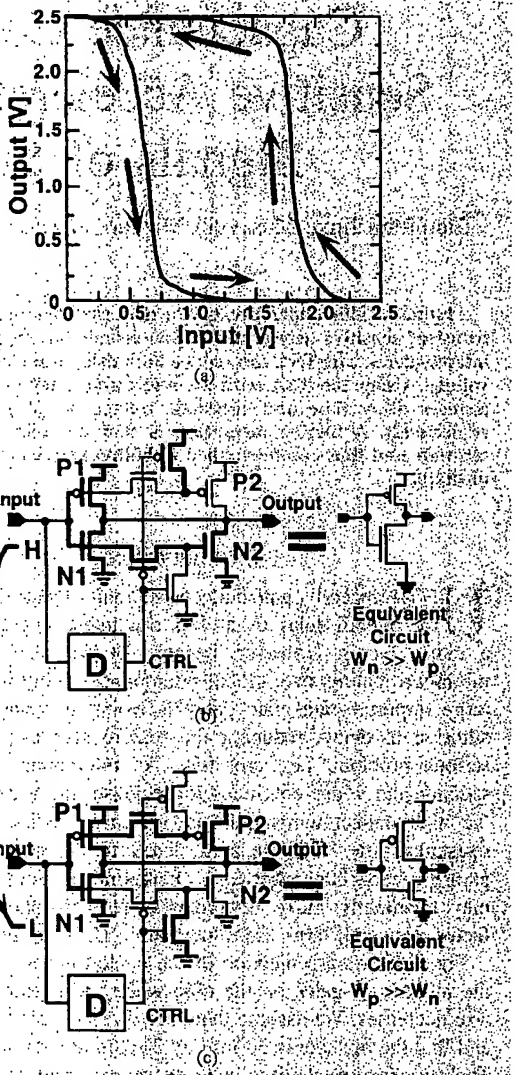


(b)

Fig. 2. Transient sensitive trigger (TST) circuit: (a) circuit configuration and (b) signal detection.

delay time, whereas a conventional inverter cannot. Unlike a conventional inverter, this circuit changes its logical threshold voltage according to the direction of the input signal transition, as illustrated in Fig. 2(b). By decreasing the size of transistors $N1$ and $P1$, and increasing the size of transistors $N2$ and $P2$, the logical threshold voltage can be set at between 0 and 1.25 V during the input rise interval, and between 1.25 and 2.5 V during the input fall interval. This results in fast detection of the signal voltage transition. Here, we assume the supply voltage is 2.5 V. Fig. 3(a) shows the simulated voltage transfer characteristics of TST. As the graph indicates, this circuit has hysteresis. When the input voltage goes from low to high, the logical threshold voltage remains low; when the input voltage goes from high to low, the logical threshold voltage stays high.

Fig. 3(b) and (c) shows how the TST transistors work at the input rise interval and the input fall interval, respectively. Transistors drawn in boldface lines represent active devices. When the input potential increases, transistors $P1$, $N1$, and



(a)

(b)

(c)

Fig. 3. Operation of TST. (a) simulated voltage transfer characteristics, (b) input rise interval, and (c) input fall interval.

$N2$ form a pseudo-inverter. In Fig. 3(b), since transistors $N1$ and $N2$ fit together to create one very wide pull-down NMOS transistor, they cause the overall logical threshold of the circuit to decrease. The lower half of circuit D consists of a Schmitt-trigger circuit and an inverter. After completion of the transition, circuit D, which controls the upper half of the circuit, changes its control signal. When the control signal changes, transistor $P2$ is activated to act as a pull-up device, while transistor $N2$ is deactivated. When the potential of the input falls, as shown in Fig. 3(c), $N1$, $P1$, and $P2$ act as a pseudo-inverter, and both transistors $P1$ and $P2$ behave like a large pull-up PMOS device. As a result, the logical threshold increases.

B. SPICE Simulation

Fig. 4 shows the signal waveforms on a 20-mm interconnect which were obtained in simulation employing parameters of

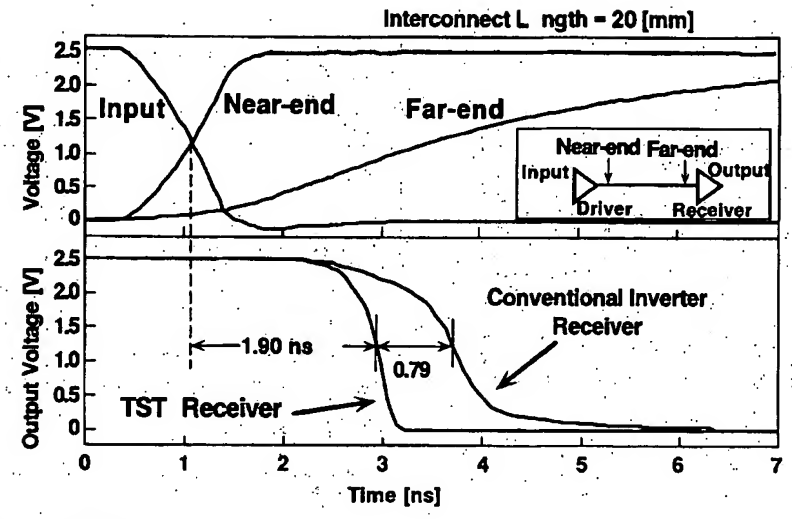


Fig. 4. Simulated interconnect waveforms.

a 0.25-μm CMOS and 1-μm pitch interconnect technology. These waveforms are computer-simulated for distributed RC lines with an interconnect resistance of 90 Ω/mm and an interconnect capacitance of 0.184 pF/mm. The top half shows the waveforms at the input, near-end, and far-end of the driver. The lower half shows the output waveforms of two receivers, i.e., a conventional inverter and the TST. We assume the same voltage is applied to each one. In the upper half of the figure, the waveform at the far-end has a long rise time due to the large RC delay of the interconnect. This means that the voltage transition speed at the far-end cannot be improved by enhancing the current drive capability of the driver, as mentioned previously. When a conventional inverter is used as a receiver, it does not react until the far-end voltage crosses the center line of the supply voltage V_{DD}. If the proposed TST receiver is placed at the far-end of the wire, it reduces the delay time by 0.79 ns, or 30%, compared to that of a conventional inverter.

The TST is much faster than a conventional inverter. On the other hand, its noise margin is much smaller. This means that in a noisy environment, the TST may not function properly. If we want to reduce delay and increase the noise margin simultaneously, another approach must be taken. That is, in addition to replacing the receiver, the wire voltage must also be manipulated during the signal transition period.

III. Transient Sensitive Accelerator (TSA) Circuit

A. Concept

As mentioned in the first section, both the delay time and crosstalk voltage should be addressed in the event of a highly resistive interconnect. As a means of doing so, we developed a new circuit, which we call the transient sensitive accelerator (TSA) circuit. Fig. 5(a) explains the basic concept of the TSA. In this figure, an interconnect is modeled by distributed RC circuits. The TSA is connected to the interconnect at some point. It receives data from this point and, after some processing, returns some information to the same point. Fig. 5(b) shows the timing diagram of the TSA operation. The interconnect voltage is assumed to have a long rise and fall time stemming from the large RC constant. As described before, the TST senses the transition of the interconnect voltage at an early stage while the Schmitt-trigger detects the change at the end of the transition. This timing difference in the sensing can be utilized as an acceleration period if we design a circuit that turns on during the interval. This would cause the voltage level of the wire to rise to the final value more rapidly during the transition period. In the same way, a circuit that maintains the interconnect voltage during a steady state can be designed. Since the main purpose of this circuit is to prevent the TST from reacting to a small voltage fluctuation, it slightly delays the signal detection of the TST.

B. Implementation

Fig. 6 shows the implementation of the ideas described above. The overall driving configuration is composed of two drivers, an interconnect, two receivers, and the newly proposed TSA. It is assumed that a long interconnect such as a bus line is used for the bidirectional signal. The TSA consists of a TST, clamp transistors, and acceleration transistors. Crosstalk voltage is usually minimized at the near-end, where the voltage is strongly influenced by the driver; however, it is maximized at the far-end, where influence from the driver is weak. Considering that the signal travels in both directions on the interconnect, it seems appropriate to place the TSA at the midpoint on the wire.

C. Operation of TSA

Fig. 7 illustrates the operation of the TSA. Actually, the Schmitt-trigger and inverter shown in the figure are not necessary because both are included in the TST, as previously shown in Fig. 2. However, we include them in Fig. 7 to facilitate understanding of the operation. In a steady state, the interconnect

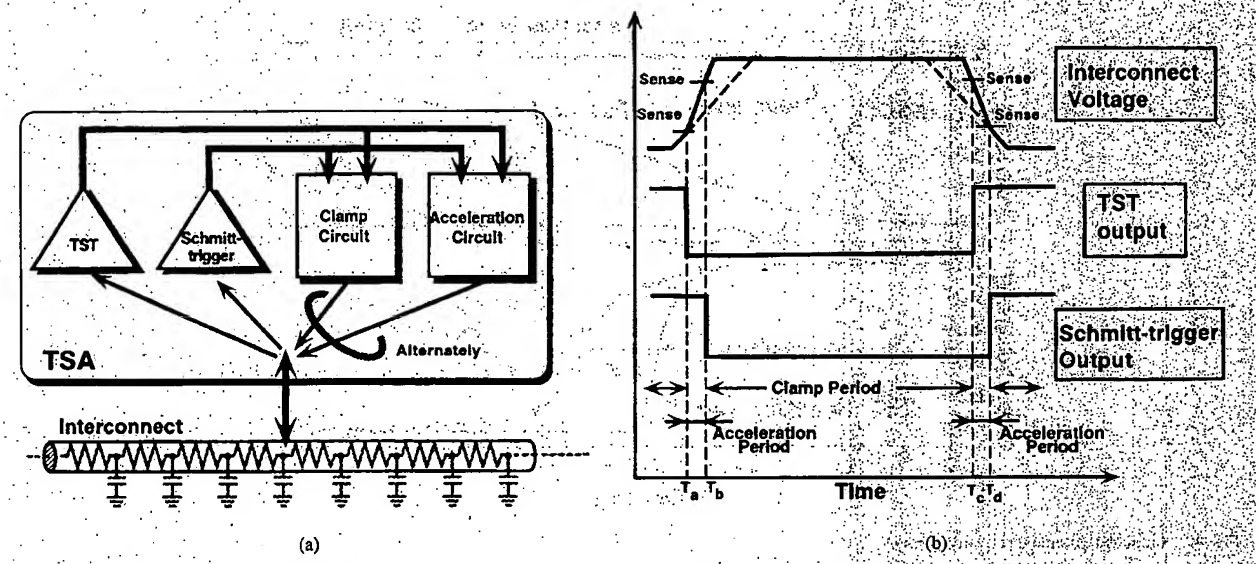


Fig. 5. Concept of transient sensitive accelerator (TSA) circuit: (a) basic concept of TSA and (b) timing diagram for the operation.

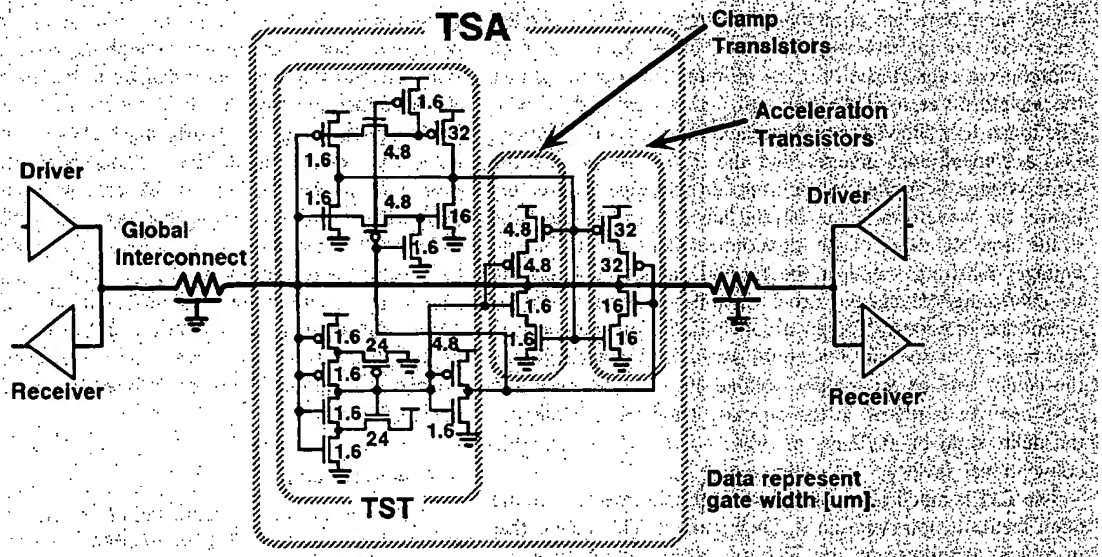


Fig. 6. Transient sensitive accelerator (TSA) circuit.

is connected to the ground or supply voltage through serially stacked clamp transistors. During the transition interval, the TST senses the transition at the early stage of the interval and changes its output. As a result, the path through the clamp transistors disappears, while the stacked acceleration transistors form another path. This path prompts the wire voltage to change quickly—in other words, it accelerates the voltage transition. The clamp transistors and the acceleration transistors work alternately. The clamp transistors work in the steady state and the acceleration transistors are turned on during the transition interval.

D. Delay Reduction by TSA

Fig. 8 illustrates a cross-sectional view model of the interconnect structure. In this model, capacitances C_1, C_2, and C_3 are approximated by using Sakurai's model [2]. We simulated delay time using the π models of distributed RC wire [3]. The delay is the simulated value under the worst voltage conditions, where the voltages of the two neighboring interconnects and the upper interconnect change simultaneously on opposite sides of the center wire. An inverter is used as a receiver. The delay times of the driving configuration, with and without using the TSA are compared. The TSA is placed at the midpoint of the interconnect. Fig. 9 shows the simulated waveforms. When the TSA is not used, the time between the input and output is approximately 9 ns due to the long rise time of the wire. When the TSA is used, an interval of 6.4 ns is achieved. The improvement corresponds to a 29% reduction. At the midpoint, the with-TSA waveform has a longer rise time until the TST reaches its logical threshold voltage. However,

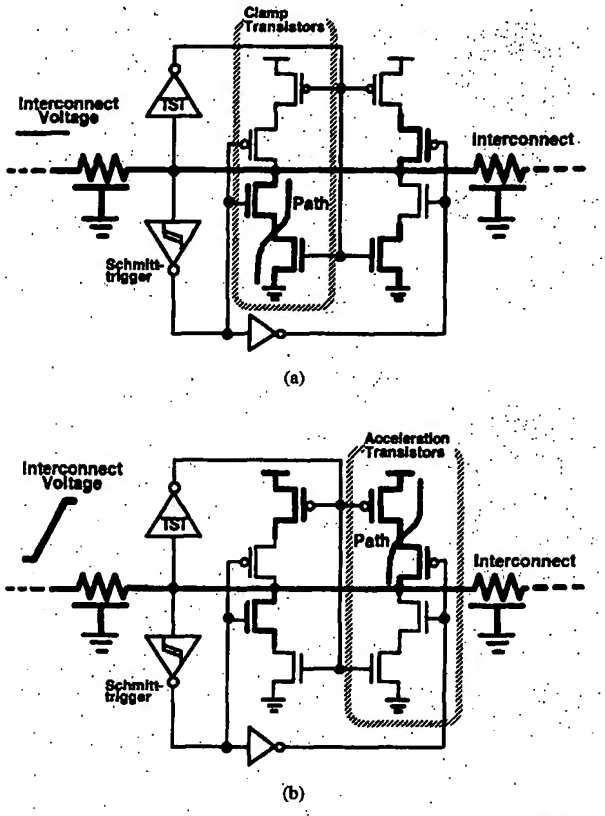


Fig. 7. Operation of TSA: (a) steady state (clamp), (b) transition (acceleration).

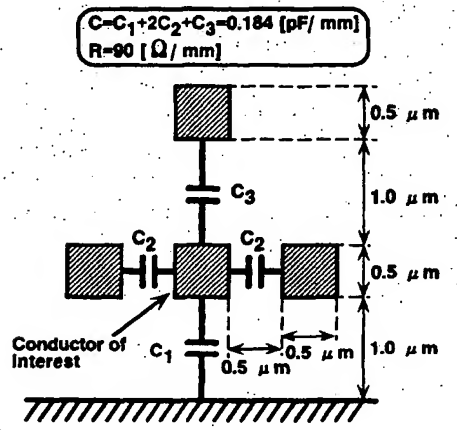


Fig. 8. Model of interconnect structure.

once this is reached, the midpoint voltage quickly goes to the V_{DD}. Note that this simulation was conducted under the worst voltage conditions. The time required could be reduced if neighboring wires were to swing on the same side of the center wire.

Fig. 10 shows the delay reduction achieved with the new circuit. As the graph indicates, the TSA reduces delay when

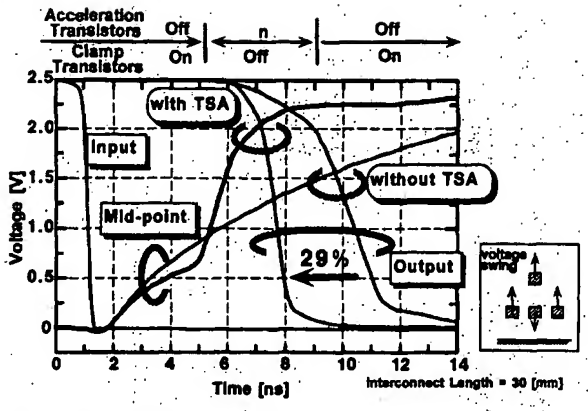


Fig. 9. Delay reduction by TSA.

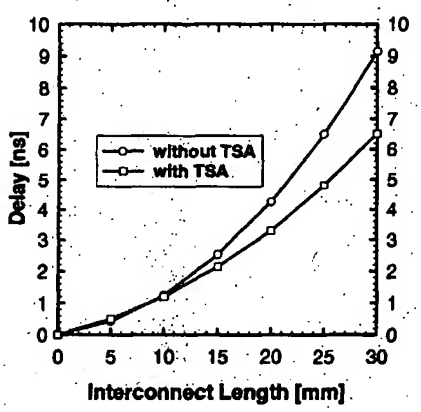


Fig. 10. Delay improvement.

interconnect length exceeds 10 mm. This means that the breaking point of this circuit in terms of delay is 10 mm.

E. Crosstalk Reduction with TSA

Fig. 11 shows the reduction in crosstalk voltage achieved by using the TSA. In general, crosstalk voltage implies parasitic capacitance interaction between neighboring interconnects. In this case, the crosstalk voltage is the simulated value under the voltage conditions where the voltages of the two interconnects and the upper interconnect change simultaneously. The origin of the horizontal axis is assumed to be at the near-end of the wire and the 30-mm position is at the far-end of the wire. By placing the TSA at the midpoint, crosstalk voltage at the far-end is reduced from 0.61 to 0.49 V—a 20% reduction.

IV. Conclusion

We have proposed a new circuit, the Transient Sensitive Accelerator (TSA) circuit, which can be used for highly resistive interconnects. Using this circuit on a 30-mm wire reduces the delay time by 29% and the crosstalk voltage by 20%. The circuit also operates in self-time and thus can be applied to bidirectional signal communication.

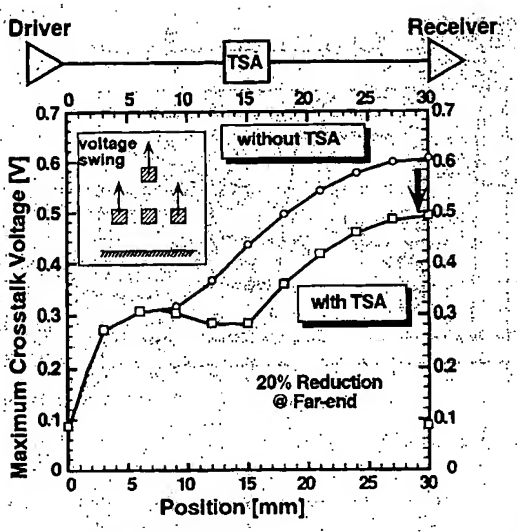


Fig. 11. Crosstalk reduction by TSA.

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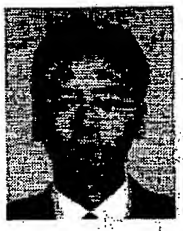
Tomofumi Iima was born in Takamatsu, Japan, on April 25, 1969. He received the B.S. and M.S. degrees in electronic engineering from Toyohashi University of Technology, Aichi, Japan, in 1992 and 1994, respectively.

He joined the System ULSI Research Laboratory, Microelectronics Research Laboratories of NEC Corporation, Kanagawa, Japan, in 1994. His research interests include high-speed microprocessor LSI's.



Masayuki Mizuno (M'95) was born in Kobe, Japan, on August 11, 1967. He received the B.S. and M.S. degrees in electronic engineering from Osaka University, Osaka, Japan, in 1991 and 1993, respectively.

In 1993 he joined the System ULSI Research Laboratory, Microelectronics Research Laboratories of NEC Corporation, Kanagawa, Japan, where he has been engaged in the research and development of high speed and low-power signal processor LSI's. His current research interests include VLSI architecture of portable communication systems, and high-speed and low-power circuit techniques.

Mr. Mizuno is a member of the Institute of Electronics, Information and Communication Engineering of Japan.

Tadahiko Horiuchi received the B.S. and M.S. degrees in nuclear engineering from Kyoto University, Japan, in 1981 and 1983, respectively. He received the doctor degree in electrical engineering from Tohoku University in 1993.

He joined NEC Corporation in 1983. From 1983, he was engaged in the research and development of MOS devices, especially on hot carrier effects of sub-micrometer MOSFET's. From 1986 to 1992, he worked on the process integration of Bipolar-CMOS device having a 0.8 μm and 0.5 μm design rule. From 1990 to 1991, he was a Visiting Scholar at the University of California, Berkeley, doing the research on reliability issues in VLSI's. He is currently working on the process integration of 0.25 μm CMOS device. His present interests are modeling hot carrier effects and the scaling issues for 0.1 μm MOSFET's.

Dr. Horiuchi is a member of the Japan Society of Applied Physics.

Masakazu Yamashina (M'87) received the B.S. and M.S. degrees from the Department of Electrical Engineering, Tokyo Institute of Technology, Tokyo, Japan, in 1982 and 1984, respectively and the Dr. Eng. degree in electrical engineering from the Tokyo Institute of Technology in 1995.

He joined the NEC Corporation, Kawasaki, Japan, in 1984. He was engaged in the research and development of CMOS video signal processor (VSP) LSI and BiCMOS DSP LSI's. During a leave from NEC in 1989–1990, he studied improving algorithms for autonomous robots at Stanford University, Stanford, CA. His current research interests include high-speed microprocessors and high-speed circuit techniques.

Dr. Yamashina is a member of the Institute of Electronics, Information and Communication Engineers of Japan.